

REMARKS

Amendments to the specification have been made and are submitted herewith in the attached Marked-up Specification. A clean copy of the specification and a marked-up version showing the changes made are attached herewith. The claims have been amended in the attached Amendment. All amendments have been made to place the application in proper U.S. format and to conform with proper grammatical and idiomatic English. The drawings have been amended to clearly label the blocks. However, it is noted that drawings were previously submitted on May 28, 2002 with English translations to the drawings. None of the amendments herein are made for reasons related to patentability. No new matter has been added.

This application is now in condition for allowance, as previously indicated by the Examiner.

In the unlikely event that the transmittal letter is separated from this document and the Patent Office determines that an extension and/or other relief is required, Applicants petition for any required relief including extensions of time and authorizes the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to **Deposit Account No. 03-1952** referencing docket no. 449122022800. However, the Commissioner is not authorized to charge the cost of the issue fee to the Deposit Account.

Respectfully submitted,

Dated: May 11, 2004

By: 

Kevin R. Spivak
Registration No. 43,148

Morrison & Foerster LLP
1650 Tysons Boulevard, Suite 300
McLean, VA 22102
Telephone: 703-760-7762
Facsimile: 703-760-7777

Description
SYSTEM AND METHOD FOR GENERATING A TRIGGER
SIGNAL BASED ON THE CURRENT DIFFERENTIAL PROTECTION METHOD
AND ARRANGEMENT

5 ~~Method for generating a trigger signal according to the~~
~~current differential protection principle and current~~
~~differential protection arrangement~~

CLAIM FOR PRIORITY

10 This application claims priority to German Application
No. 10106279.6 which was published in the German language
on February 5, 2001, the contents of which are hereby
incorporated by reference.

15

TECHNICAL FIELD OF THE INVENTION

The invention relates to a system and method for
generating a trigger signal according to, and in
particular, to generating a trigger signal based on the
20 current differential protection principle in the case of a
fault on a section of an electrical power supply system, in
which differential current values are monitored with regard
to exceeding a predetermined lower limit value of the
differential current (differential current limit value) and
25 also with regard to exceeding stabilization current values
weighted with a characteristic curve factor, and the
trigger signal is generated if positive results of the two
instances of monitoring are present simultaneously.

BACKGROUND OF THE INVENTION

~~A method of this type is disclosed in the~~ German patent specification DE 44 36 254 C1. ~~In this known method,~~1
discloses current transformers are used to detect currents
5 at the ends of a section of an electrical power supply system which is to be monitored with regard to the occurrence of an internal fault. In the known method, the currents obtained by means of the current transformers are converted, in a measured value preprocessing device, into
10 root-mean-square-value-proportional measurement quantities, with which differential and stabilization current values are obtained. In order to detect a fault on the section of a power supply system that is to be monitored, differential current values are monitored with regard to exceeding a
15 predetermined lower limit value of the differential current (differential current limit value) and with regard to exceeding stabilization current values weighted with a characteristic curve factor;~~the.~~ The trigger signal is generated if positive results of the two instances of
20 monitoring are present simultaneously.

In the known method, special precautions have to be taken to guard against incorrect triggering on account of saturation phenomena in the current transformers. This is
25 because, under certain circumstances, current transformers transform the measured values completely satisfactorily only for in each case a limited short time span of each period, because they enter into saturation in the case of relatively large current values. As a result of the
30 saturation phenomena in the current transformers,

intrinsically external faults with regard to the section to be monitored may mistakenly be classified as internal faults, which can then lead to undesirable triggering. In order to prevent that, ~~in the known method according to the~~
 5 ~~current differential protection principle~~this, care is taken to ensure that the outputting of a trigger signal is blocked after an external fault has been ascertained in the state of unsaturated current transformers. In this case, the blocking is not performed for a fixedly predetermined
 10 time, but rather is effected for a predetermined time duration starting from an instant which depends on the respective conditions. After this time duration has elapsed, the known method can then respond again to an internal fault.

SUMMARY OF THE INVENTION

~~The invention is based on the object of proposing a~~ The invention relates to a system and method for generating a trigger signal, and in particular, to generating a trigger
 20 signal based on the current differential protection principle in the case of a fault on a section of an electrical power supply system, in which differential current values are monitored with regard to exceeding a predetermined lower limit value of the differential current
 25 (differential current limit value) and also with regard to exceeding stabilization current values weighted with a characteristic curve factor, and the trigger signal is generated if positive results of the two instances of monitoring are present simultaneously.

The invention also discloses a system and method for
generating a trigger signal according to the current
differential protection principle which can be used to
generate a trigger signal rapidly and reliably in the case
5 of an internal fault - ~~whilst~~while avoiding incorrect
triggering in the case of external faults with transformer
saturation.

~~In order to achieve this object, in the case of a method of~~
10 ~~the type specified in the introduction, according to~~ In
one embodiment of the invention, the differential current
values and the stabilization current values are calculated
with instantaneous values of the currents detected at the
electrical power supply system, and a first measurement
15 quantity, which is proportional to the differential
quotient of the stabilization current with respect to time,
is formed and checked in an evaluation operation to
determine whether ~~this~~the first measurement quantity
exceeds a predetermined limit value of the differential
20 quotient of the differential current with respect to time
(differential current quotient limit value); ~~furthermore,~~
a. A second measurement quantity, which is proportional to
the differential quotient of the differential current with
respect to time, is formed and checked in a further
25 evaluation operation to determine whether the second
measurement quantity exceeds the differential current
quotient limit value, and the trigger signal is generated
if the two evaluation operations produce positive results
at the same time as the two instances of monitoring.

An ~~essential advantage of the method according to the invention is seen in the fact that, in the first place,~~ the computational complexity can be kept comparatively low by virtue of the processing of instantaneous values of the currents detected on the electrical power supply system. This is also fostered by the fact that the evaluation operations proceed relatively simply in the method according to the invention, with the result that overall the computational complexity is comparatively low. On the other hand, with the method according to the invention, there is the advantageous possibility of performing the computation operations at comparatively short intervals, without having to use a relatively large data processing device.

In order to preclude, with particularly high certainty, incorrect triggering in the case of external faults with accompanying saturation of the current transformers, in a ~~further configuration~~ another embodiment of the ~~method according to the invention,~~ a check is made to determine whether the first measurement quantity is greater than the second measurement quantity, and, if appropriate, the trigger signal is generated.

Furthermore, in order to further increase the reliability of the ~~method according to the invention,~~ it ~~has proved to be advantageous~~ is preferable if a check is made to determine whether the second measurement quantity exceeds the first measurement quantity weighted with the

characteristic curve factor, and, if appropriate, the trigger signal is generated.

In order, ~~in the method according to the invention,~~ to
5 prevent an apparent fault location outside the section from
being identified on account of impedance differences in the
supplies in the case of a fault on the section of the
electrical power supply system that is to be monitored, in
~~a further advantageous~~another embodiment of ~~the method~~
10 ~~according to the invention,~~ the smallest value of the
stabilization current is determined in each case in a time
range in which the first measurement quantity becomes less
than zero, and its largest value is determined in each case
in a time range in which the first measurement quantity
15 becomes greater than zero, and a check is made to determine
whether the stabilization current is greater than K_{MIN}
times the smallest value of the stabilization current,
where $1 < K_{MIN} < \sqrt{2}$, and 0.5 times the value of the largest
value, and, if appropriate, the trigger signal is
20 generated.

In an ~~advantageous~~still another embodiment of ~~the~~
~~method according to the invention,~~ the trigger signal is
generated if the evaluation operations and the instances of
25 monitoring have yielded positive results N_s times in
succession, where N_s is freely selectable. As a result, it
is possible to effect high-speed triggering if N_s is chosen
to be very small, e.g. $N_s = 1$ or $N_s = 2$.

If high-speed triggering cannot be achieved ~~with the method according to the invention~~, then it is advantageous that, in the absence of N_s results, the trigger signal is generated when at least the instances of monitoring have
5 produced positive results N_z times, where $N_s \ll N_z$.

In the ~~method according to the invention~~, in order to avoid incorrect triggering, it is ~~furthermore regarded as advantageous~~preferable if, in the absence of a trigger
10 signal, an internal inhibit signal is generated if the first measurement quantity is greater than the limit value of this quantity, furthermore the second measurement quantity is less than the instantaneous value - weighted with the k factor - of the first measurement quantity and,
15 at the same time, the instantaneous value of the stabilization current is greater than a limit value, a first reweighted limit value, a second reweighted limit value, and a comparison value calculated as mean value from previous values.

20

The invention ~~furthermore~~also relates to a current differential protection arrangement for a section of an electrical power supply system having a measured value preprocessing device, in which respective differential
25 current values and stabilization current values respectively assigned thereto are formed continuously from currents detected at the ends of the section, having an evaluation device connected downstream of the measured value preprocessing device, in which evaluation device the
30 differential current is checked to determine whether it

exceeds a predetermined differential current limit value, and having a logic circuit, which, on the input side, is connected to the evaluation device and has an output for outputting a trigger signal. Such a current differential protection arrangement is described in the German patent specification DE 44 36 254 C1, which was already dealt with in the introduction.

In order, with such a current differential protection arrangement, to be able to obtain trigger signals rapidly and reliably in the case of an internal fault on the section of an electrical power supply system that is to be monitored, according to an embodiment of the invention, the measured value preprocessing device is designed in such a way that it generates differential current instantaneous values and stabilization current instantaneous values, ~~furthermore.~~ Furthermore, a first limit value stage is arranged downstream of a first differentiator, to which stabilization current instantaneous values are applied, which limit value stage is also connected to a differential current quotient limit value transmitter on the input side, ~~also a.~~ A second limit value stage is arranged downstream of a second differentiator, to which differential current instantaneous values are applied, which limit value stage is also connected to the differential current quotient transmitter on the input side, and the logic circuit is arranged downstream of the limit value stages and generates the trigger signal when output signals of the limit value stages are present.

~~Further~~ In further advantageous configurations of this current differential protection arrangement ~~emerge from~~ ~~claims 9 to 13, where it should be pointed out that,~~ the construction of the current differential protection
 5 arrangement according to the invention is expediently effected overall by means of a data processing device.

BRIEF DESCRIPTION OF THE DRAWINGS

For ~~thea~~ a further explanation of the ~~method according~~
 10 ~~to the invention and of the current differential protection~~ arrangement according to the invention,

Figure 1 represents a block diagram for describing the sequence of an exemplary embodiment of the method
 15 according to the invention, ~~and~~ .

Figure 2 represents an embodiment of a logic circuit of the block diagram in accordance with Figure 1.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Figure 1 shows a section E of a power supply system N, which section is to be monitored for faults and is bounded by current transformers W1 and W2. By means of the current transformers W1 and W2, secondary currents i1 and i2 which
 25 are proportional to the currents through the primary windings of ~~said~~ the transformers are obtained and are fed to a measured value preprocessing device MV with evaluation device AW arranged downstream.

~~Said~~ The measured value preprocessing device MV ~~contains~~ includes, inter alia, low-pass filters which eliminate changes in the currents i_1 and i_2 which are caused for example by external electromagnetic influencing.

5 Furthermore, differential current instantaneous values i_d are formed in the measured value preprocessing device MV in accordance with equation (1) below.

$$i_d = |\sum (i_1, i_2)| \quad (1)$$

10

Stabilization current instantaneous values i_s are also generated in the measured value preprocessing device MV in accordance with equation (2) below.

$$15 \quad i_s = \sum |i_1| |i_2| \quad (2)$$

According to the theory, through consideration of the currents i_d and i_s , a fault-free section E can be inferred if the differential current i_d is zero, ~~—a.~~ a. A fault on the
 20 section E is given when the differential current i_d has ~~exactly~~ the same magnitude as the stabilization current i_s . In practice, however, the conditions are considerably more complicated because, during the detection of the secondary currents i_1 and i_2 , measurement errors occur as a result of
 25 the use of the current transformers W1 and W2. These measurement errors are particularly large when the current transformers W1 and W2 enter into saturation, which may be the case when there is a short circuit in the power supply system N with accompanying short-circuit currents.

In practice, therefore, it is assumed in the case of a fault on the section E that then

$$5 \quad id > idg \quad (5)$$

$$id > K \cdot is \quad (6)$$

In this case, idg denotes a limit value of the differential current id . K designates a characteristic curve factor whose magnitude, in a known manner, lies between zero and 1. This characteristic curve factor K takes account of the fact that measurement errors during the detection of the currents i_1 and i_2 can become larger with increasing current on the section E and that normal load currents flowing via the section E can be superposed on the fault current and differential impedances of connected lines can bring about phase differences. Under the customary operating conditions of the power supplies, adequate stability of a current differential protection arrangement working with these criteria can be achieved if the differential current limit value idg and the characteristic curve factor K are set high enough; ~~however~~. However, it ~~must~~should be taken into account that a satisfactory sensitivity for the application ~~must be~~is ensured by setting these quantities low enough.

In the exemplary embodiment according to Figure 1, equations (5) and (6) are taken into account by virtue of the fact that a comparison arrangement VA1 of the

evaluation device AW is connected by an input to an output A1 of the measured value preprocessing device MV, ~~said~~the output carrying differential current instantaneous values ~~id, the~~. The comparison arrangement VA1 is connected by its
 5 other input to a limit value transmitter G1g, which, at its output, outputs a measurement quantity proportional to the differential current limit value igd. Moreover, a further comparison arrangement VA2 is connected by one of its inputs to the output A1 of the measured value preprocessing
 10 device MV, ~~a~~. A further input of the ~~said~~ further comparison arrangement VA2 is connected to a further output A2 of the measured value preprocessing device MV via a weighting stage V, ~~stabilization~~. Stabilization current instantaneous values is occur at ~~said~~the output A2.

15

If equation (5) is satisfied, then the comparison arrangement VA1 outputs an actuation signal to an input E1 of a logic circuit L arranged downstream of the evaluation device AW. If equation (6) is satisfied, then the further
 20 comparison arrangement VA2 supplies an actuation signal to an input E2 of the logic circuit L.

In the exemplary embodiment illustrated, the logic circuit L, whose function will be described in detail
 25 below, does not already generate a trigger signal A when actuation signals of the comparison arrangements VA1 and VA2 are present at the two inputs E1 and E2, rather further conditions - described in more detail below - must also be met for the outputting of the trigger signal A.

30

In order to check the further conditions, a first differentiator DS is connected to the further output A2 of the measured value preprocessing device MV, which differentiator generates, at its output, a first measurement quantity isd , which is proportional to the differential quotient of the stabilization current i_s with respect to time. This first measurement quantity isd is fed to one input of a first limit value stage G_s , whose other input is connected to a differential current quotient limit value transmitter G_l . ~~Said~~The transmitter G_l prescribes a limit value of the differential quotient of the differential current i_d with respect to time, which is referred to below for short as differential current quotient limit value $igdl$. If the first measurement quantity isd is greater than the differential current quotient limit value $igdl$, that is to say if the relationship (7)

$$isd > igdl \quad (7)$$

holds true, then the first limit value stage G_s outputs, on the output side, a further actuation signal to an input E3 of the logic circuit L.

Moreover, a second differentiator D_d is arranged downstream of the first output A1 of the measured value preprocessing device MV, which differentiator generates, at its output, a second measurement quantity idd , which corresponds to the differential quotient of the differential current i_d with respect to time. This second

measurement quantity i_{dd} is present at an input of a second limit value stage G_d , whose other input is likewise connected to the first transmitter G_1 . If the second measurement quantity i_{dd} is greater than the differential
 5 current limit value i_{gd1} , that is to say if equation (8) below

$$i_{dd} > i_{gd1} \quad (8)$$

10 holds true, then ~~said~~the second limit value stage G_d outputs an additional actuation signal to an input E_4 of the logic circuit L .

By virtue of the additional signals at the inputs E_3
 15 and E_4 , the ~~method according to the invention~~ has already become comparatively secure with regard to undesirable incorrect triggering, ~~however.~~ However, it can be configured even more securely in terms of its function and with regard to the avoidance of incorrect triggering if a
 20 further relationship (9) is taken into account, this being presented below.

$$i_{sd} > i_{dd} \quad (9)$$

25 In Figure 1, to that end a first comparator K_1 is provided, which is connected by one of its inputs to the output of the second differentiator D_d and to which the second measurement quantity i_{dd} is thus applied; ~~a.~~ A further input of the first comparator K_1 is connected to
 30 the output of the first differentiator D_s and therefore has

the first measurement quantity i_{sd} applied to it. If relationship (9) above is fulfilled, then the first comparator K1 outputs an additional actuation signal to an input E5 of the logic circuit L.

5

A second comparator K2 is connected by its output to a further input E6 of the logic circuit L, ~~said~~the comparator serving for the evaluation of relationship (10) below.

$$10 \quad i_{dd} > K \cdot i_{sd} \quad (10)$$

For this purpose, the second comparator K2 is connected by one input to the output of the second differentiator Dd. A further input of the second comparator
15 K2 is connected to the output of the first differentiator Ds via an evaluation stage U1. If condition (10) is met, then the second comparator K2 outputs an actuation signal to the input E6 of the logic circuit L.

20 Furthermore, in the exemplary embodiment according to Figure 1, a test circuit P is provided, which is connected by its input to the output of the second differentiator Dd and checks whether the second measurement quantity i_{dd} is greater than zero. If this is the case, then it outputs a
25 pulse to an input E7 of the logic circuit L. A further input E8 of the logic circuit L is connected to an output of a comparator stage VS. The stabilization current i_s is applied to one input of ~~said~~the comparator stage, while its other input is connected to a determination device U via a
30 weighting device BE, ~~the~~ The stabilization current i_s is

applied to ~~said~~the determination device on the input side
 and ~~said~~the determination device ascertains the presently
 smallest value ismin and the largest value ismax of the
 stabilization current is. If relationship (11) below is
 5 fulfilled

$$0.5is_{max} < is > KMIN \cdot is_{min} \quad (11)$$

then the comparison stage VS outputs a signal to the logic
 10 circuit L via the input E8.

The logic circuit L additionally has inputs E11, E12,
 E13, E14 and E15. A first comparator stage V1 is connected
 to the input E11, which comparator stage, on the input
 15 side, is connected to the output A2 of the measured value
 preprocessing device MV and a second limit value
 transmitter G2g. The comparator stage V1 checks whether
 relationship (12) is complied with:

$$20 \quad is > ish \quad (12)$$

If this is the case, then an inhibit signal is output to
 the input E11.

25 The output of a second comparison stage V2 is
 connected to the input E12; ~~the~~the12. The second comparison
 stage V2 is connected by one of its inputs, via a
 translation stage U2 (factor 1/K), to the limit value
 transmitter G1g for the differential current quotient limit
 30 value idg, while the stabilization current is is applied

directly to the other input. Consequently, the following condition (13) is checked by means of the second comparison stage V2 using a first reweighted limit value idg/K :

$$5 \quad is > idg / K \quad (13)$$

If this condition and, simultaneously with a second reweighted limit value $1.5*idg$, the condition $is > 1.5*idg$ are met, then an inhibit signal occurs at the input E12 of the logic circuit L.

On the input side, a third comparison stage V3 is connected, on the one hand, to the output of the first differentiator Ds and, on the other hand, to the output of the second transmitter G2; ~~on 2.~~ On the output side, the third comparator stage V3 is connected to the input E13 of the logic circuit L and outputs to the latter an inhibit signal when the following condition (14) is met:

$$20 \quad isd > igd2 \quad (14)$$

On the input side, a fourth comparison stage V4 is connected, on the one hand, to the further output A2 of the measured value preprocessing device MV via a further translation stage U3 (factor KA) and also, on the other hand, directly to the first output A1 of the measured value preprocessing device MV. On the output side, the fourth comparison stage V4 is connected to an input E14 of the logic circuit L and outputs an inhibit signal to this input if the following relationship (15) is satisfied:

$$id < KA \cdot is \quad (15)$$

Finally, a comparator device VE checks whether
 5 relationships (16) and (17) below are satisfied:

$$is > KMIN \cdot is_{min} \quad (16)$$

$$is > 0.5 \cdot is_{max} \quad (17)$$

For this purpose, on the input side, the comparison device
 10 VE is directly connected to the output A2 of the measured
 value preprocessing device MV, ~~on~~. On the output side, the
 comparison device VE is connected to the input E15 of the
 logic circuit L. In the comparator device, a calculated
 comparison value is determined by subtracting a comparison
 15 value from the root-mean-square value of the stabilization
 current isrms. The calculated comparison value is compared
 with the instantaneous value of the stabilization current
 is.

20 As revealed by Figure 2, the logic circuit L arranged
 downstream of the evaluation device AW has, on the input
 side, a plurality of AND gates UG1 to UG5, which, on the
 input side, are connected to the inputs E1 to E14 of the
 logic circuit in the manner which can be seen from Figure
 25 2. If the first measurement quantity isd is less than the
 predetermined differential current quotient limit value
 igd1 and less than the second measurement quantity idd and
 if, moreover, the second measurement quantity idd does not
 exceed ~~said~~the limit value and it is smaller than the first
 30 measurement quantity isd weighted with the characteristic

curve factor k , then an inhibit signal B is generated at the output of the AND element $UG5$ if the conditions

$$isd > igd2$$

$$5 \quad idd > k \cdot isd$$

are met and the following simultaneously holds true for the instantaneous value of the stabilization current is:

$$10 \quad is > ish$$

$$is > idg / k$$

$$is > 1.5 \cdot idg$$

$$is > im$$

15 In this case, im designates a comparison value which is calculated from previous root-mean-square values of the stabilization current is plus a threshold value. The inhibit signal B thus occurs in the case of an external fault with regard to the section E of the power supply
20 system N that is to be monitored.

The inhibit signal B is applied, on the one hand, to a further AND element $UG6$ and, on the other hand, to a counter $Z1$ - forming a high-speed stage - at its reset
25 input, so that, when the inhibit signal B occurs and there is a signal at the input $E15$, a timer ZG is reset and the counter $Z1$ is also reset. As a result, a further counter $Z2$ is activated, which acts as a timing stage and, in the event of a counter reading greater than the count Nz ,
30 predetermined by a transmitter $GZ2$, outputs a signal to an

OR element OG via a comparator VZ2 and an additional AND element UG7.

The high-speed stage by means of the counter Z1 is
5 activated if it is determined, in a comparator VZ1
connected downstream, that a counter reading which is
greater than a predetermined count Ns of a further
transmitter GZ1 has been reached in the counter Z1. In this
case, Ns is chosen to be considerably smaller than Nz. If
10 the counter reading of the counter Z1 is greater than Ns,
the trigger signal A is generated.

SYSTEM AND METHOD FOR GENERATING A TRIGGER SIGNAL BASED ON
A CURRENT DIFFERENTIAL PROTECTION METHOD AND ARRANGEMENT

Abstract

5

~~Method for generating a trigger signal according to the
current differential protection principle and current
differential protection arrangement~~

The invention relates to a method and an arrangement
10 for generating a trigger signal according to the current
differential protection principle ~~in the case of~~ when a
fault occurs on a section of an electrical power supply
system, in which differential current values and
stabilization current values are detected and monitored
15 with regard to exceeding limit values; ~~a.~~ a. A trigger signal
is generated if positive results of the instances of
monitoring are present. ~~In order, in the case of such a
method, to obtain a trigger signal reliably and certainly
in the case of a fault on the section of an electrical~~
20 ~~power supply system, according to the invention, the~~ The
differential current values ~~(id)~~ and the stabilization
current values ~~(is)~~ are calculated with instantaneous
values of the detected power supply currents as
instantaneous values. A first measurement quantity ~~(isd),~~
25 ~~which is proportional to the differential quotient of the
stabilization current (is) with respect to time, and a
second measurement quantity (idd), which is proportional to
the differential quotient of the differential current (id)
with respect to time, are formed,~~ and a check is made by
30 ~~means of evaluation to determine whether the two~~

measurement quantities ~~(isd, idd)~~ exceed a predetermined
 limit value of the differential quotient of the
 differential current with respect to time ~~(igd)~~. If the
 instances of evaluation and the instances of monitoring
 5 produce positive results, the trigger signal ~~(A)~~ is
 generated.

10

~~2000 P 23439 DE~~~~— 23 —~~~~2000 P 23439 DE~~

15

~~- 21 -~~~~2000P23439DE~~

20